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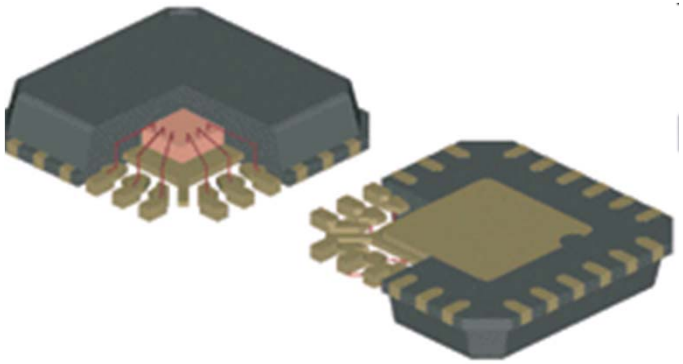
# Manufacturing and Reliability Challenges With QFN (Quad Flat No Leads)



Cheryl Tulkoff

ASQ Reliability Society Webinar

March 10, 2011

# Instructor Biography

- Cheryl Tulkoff has over 17 years of experience in electronics manufacturing with an emphasis on failure analysis and reliability. She has worked throughout the electronics manufacturing life cycle beginning with semiconductor fabrication processes, into printed circuit board fabrication and assembly, through functional and reliability testing, and culminating in the analysis and evaluation of field returns. She has also managed no clean and RoHS-compliant conversion programs and has developed and managed comprehensive reliability programs.

- Cheryl earned her Bachelor of Mechanical Engineering degree from Georgia Tech. She is a published author, experienced public speaker and trainer and a Senior member of both ASQ and IEEE. She holds leadership positions in the IEEE Central Texas Chapter, IEEE WIE (Women In Engineering), and IEEE ASTR (Accelerated Stress Testing and Reliability) sections. She chaired the annual IEEE ASTR workshop for four years and is also an ASQ Certified Reliability Engineer.

- She has a strong passion for pre-college STEM (Science, Technology, Engineering, and Math) outreach and volunteers with several organizations that specialize in encouraging pre-college students to pursue careers in these fields.

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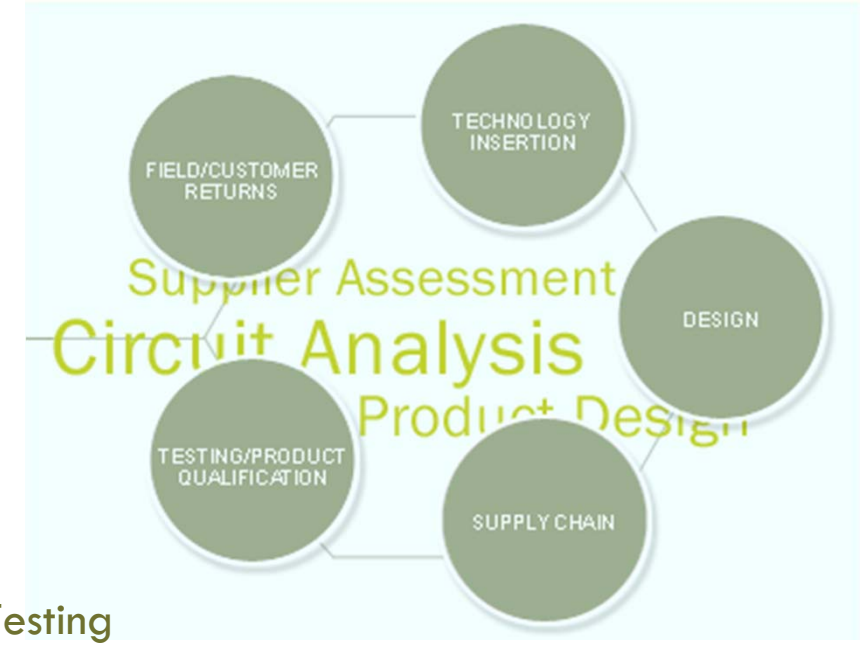
**DfR Solutions works with companies and individuals throughout the life cycle of a product, lending a guiding hand on quality, reliability and durability (QRD) issues that allows your staff to focus on creativity and ideas.**

**Our expertise in the emerging science of Electrical and Electronics Reliability Physics provides crucial insights and solutions early in product design, development and test throughout manufacturing, and even into the field.**

# Who is DfR Solutions?

- We use Physics-of-Failure (PoF) and Best Practices expertise to provide knowledge-based strategic quality and reliability solutions to the electronics industry
  - Technology Insertion
  - Design
  - Manufacturing and Supplier Selection
  - Product Validation and Accelerated Testing
  - Root-Cause Failure Analysis & Forensics Engineering




- Unique combination of expert consultants and state-of-the-art laboratory facilities

# DfR Clients

**Military / Avionics / Space**

- Rockwell Collins
- DRS
- Honeywell
- Applied Data Systems
- Mercury Computers
- Digital Receiver Technology
- Hamilton Sundstrand
- Kato Engineering
- Thales Communications
- L-3 Communications
- Innovative Concepts
- Sandia National Labs
- Crane (Eldec)
- ViaSat
- Eaton

**Automotive / Commercial Vehicle**

- General Motors
- Caterpillar
- Panasonic Automotive
- Hella Automotive
- LG Electronics
- Tyco Electronics
- TRW
- MicroHeat

**Medical**

- Biotronik
- Philips Medical
- Abbott Laboratories
- Tecan Systems
- Neuropace
- Inter-Metro
- Welch Allyn
- Guidant / Boston Scientific
- Beckman Coulter
- Applied Biosystems
- Cardinal Health
- Medtronic
- Cardiac Science

**Server / Telecom**

- Lucent Technologies
- Sun Microsystems
- Cisco Systems
- Artesyn Communications
- Corvis Communications
- Huawei (China)
- Airgo Networks
- Verigy
- Antares ATT
- Enterasys
- True Position
- HiFN
- Cedar Point
- Optics1
- Tropos Networks

**Consumer / Appliance**

- Fujitsu (Japan)
- Dell Computers
- Samsung (Korea)
- LG Electronics (Korea)
- Tubitak Mam (Turkey)
- Insinkerator
- White Rodgers
- Emerson Appliance Controls
- Therm-O-Disc
- NMB Technologies
- Shure
- Handi-Quilt
- Xerox

**Portables**

- RSA Security
- Handheld
- Kyocera
- LG Electronics

**Contract Manufacturers**

- Daeduck (Korea)
- Gold Circuit Electronics (Taiwan)
- Engent
- EIT

Industrial / Power

- Schlumberger
- Copeland
- Tennant
- Rosemount
- Branson
- Computer Process Controls
- ASCO Power
- ASCO Valve
- Astec
- Liebert
- Avansys
- Tyco Electronics
- Rainbird
- MicroMotion
- Siemens
- Barco
- Calex
- Western Geco (Norway)
- General Electric
- Ingersoll Rand
- Fusion UV
- Numatics
- Durotech
- Danaher Motion
- TallyGencom
- Vision Research
- Olympus NDT

Components

- Fairchild Semiconductor
- Maxtek
- Samsung ElectroMechanics (Korea)
- Pulse
- Teradyne
- Amphenol
- AVX
- Anadigics
- Kemet
- NIC
- Graftech
- International Rectifier

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# Selected Publications

- Epidemiological Study of SnAgCu Solder: Benchmarking Results from Accelerated Life Testing
- What I Don't Know That I Don't Know: Things to Worry About with the Pb-Free Transition
- Long-term Reliability of Pb-free Electronics
- Robustness of Ceramic Capacitors Assembled with Pb-Free Solder
- Failure Mechanisms in LED and Laser Diodes
- Microstructure and Damage Evolution in Pb-Free Solder Joints
- Improved Methodologies for Identifying Root-Cause of Printed Board Failures
- Reliability of Pressure Sensitive Adhesive Tapes for Heat Sink Attachment
- Failure Mechanisms in Electronic Products at High Altitudes
- Determining the Lifetime of Conductive Adhesive / Solder Plated Interconnections
- Issues in Long-Term Storage of Plastic Encapsulated Microcircuits
- Effect of PWB Plating on the Microstructure and Reliability of SnAgCu Solder Joints
- A Demonstration of Virtual Qualification for the Design of Electronic Hardware
- Solder Failure Mechanisms in Single-Sided Insertion-Mount Printed Wiring Boards
- Finite Element Modeling of Printed Circuit Boards for Structural Analysis

# DfR Resources and Equipment

**Electrical**

- Oscilloscopes
  - Digital
  - Analog
- Curve Tracers
  - Digital
  - Analog
- Partial Discharge Detector
- Capacitance Meters
- Low Resistance Meters
- High Resistance Meters
- High Voltage Power Supplies (Hi-Pot)

**Testing**

- HALT
- Temperature Cycling
- Thermal Shock
- Temperature/Humidity
- Vibration
- Mechanical Shock / Drop Tower
- Mixed Flowing Gas
- Salt Spray
- Capacitor Testing (Ripple Current)

**Material Analysis**

- X-ray
- Acoustic Microscopy
- Infrared Camera
- Metallographic Preparation
- Stereoscope
- Optical Microscope
- Scanning Electron Microscope
- Energy Dispersive Spectroscopy
- Ion Chromatography
- FTIR (Solid / Film / Liquid)
- Thermomechanical Analyzer
- SQUID Microscopy
- Xray Diffraction
- Focused Ion Beam Imaging
- XPS

**Other**

- Circuit Simulation
- Finite Element Analysis (FEA)
- Computational Fluid Dynamics
- Reliability Prediction (Physics of Failure)

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# Knowledge and Education (Website)

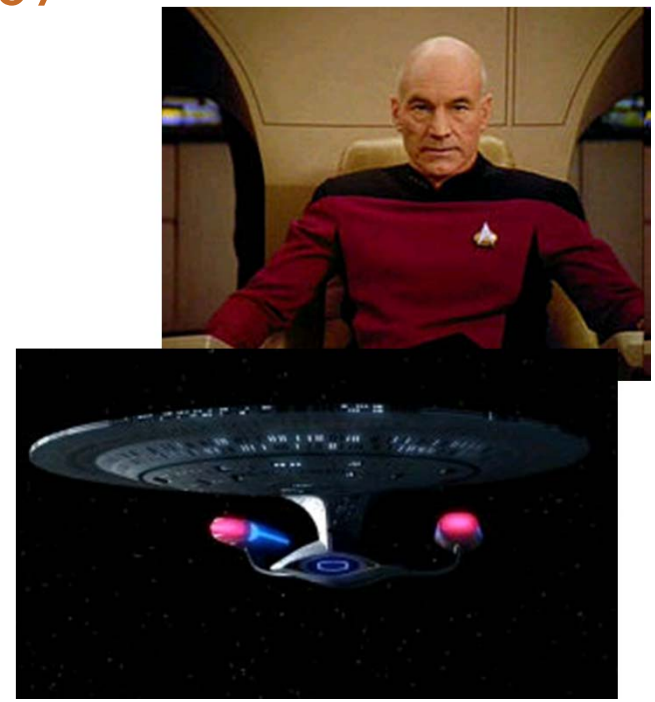
- Let your staff learn all day / every day

## E-LEARNING

- Scholarly articles
- Technical white papers
- Case studies
- Reliability calculators
- Online presentations

# QFN as a 'Next Generation' Technology

- What is 'Next Generation' Technology?
  - Materials or designs currently being used, but not widely adopted (especially among hi-rel manufacturers)
- Carbon nanotubes are not 'Next Generation'
  - Not used in electronic applications
- Ball grid array is not 'Next Generation'
  - Widely adopted



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# Introduction (cont.)

- Why is knowing about 'Next Generation' Technologies important?
- These are the technologies that you or your supply chain will use to improve your product
  - Cheaper, Faster, Stronger, 'Environmentally-Friendly', etc.
- And sooner then you think!

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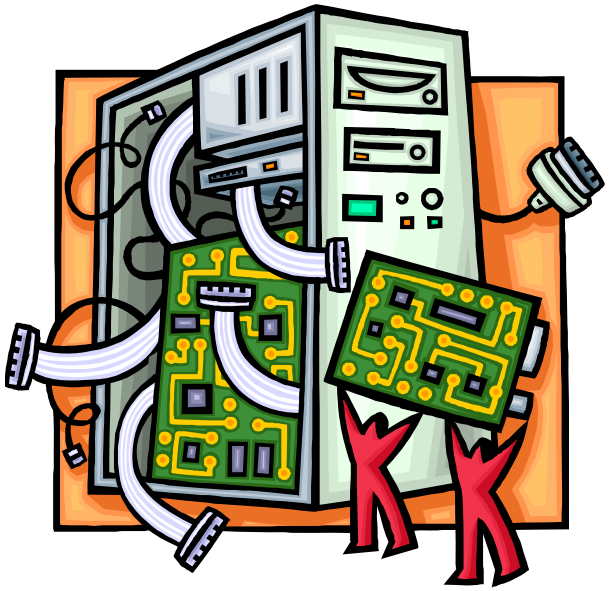
# Reliability and Next Generation Technologies

- One of the most common drivers for failure is inappropriate adoption of new technologies
  - The path from consumer (high volume, short lifetime) to high rel is not always clear
- Obtaining relevant information can be difficult
  - Information is often segmented
  - Focus on opportunity, not risks
- Can be especially true for component packaging
  - BGA (Ball Grid Array), flip chip, QFN (Quad Flat No Lead)



# Component Packaging

- Most of us have little influence over component packaging
  - Most devices offer only one or two packaging styles

- Why should you care?
  - Poor understanding of component qualification procedures
  - Who tests what and why?

# Component Testing

- Reliability testing performed by component manufacturers is driven by JEDEC
  - JESD22 series (A & B)
- Focus is almost entirely on die, packaging, and 1st level interconnections (wire bond, solder bump, etc.)
- Only focus on 2nd level interconnects (solder joints) is JESD22-B113 Cyclic Bend Test
  - Driven by cell phone industry
  - They have little interest in thermal cycling or vibration!

# 2nd Level Interconnect Reliability

- IPC has attempted to rectify this through IPC-9701
- Two problems
  - Adopted by OEMs; not by component manufacturers
  - Application specific; you have to tell them the application (your responsibility, not theirs)
- The result
  - An increasing incidence of solder wearout in next generation component packaging

# Solder Wearout in Next Generation Packaging

## Performance Needs

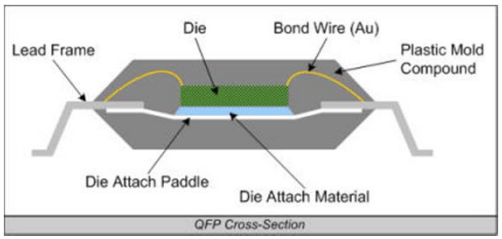
- Higher frequencies and data transfer rates
  - Lower resistance-capacitance (RC) constants
- Higher densities
  - More inside less plastic
- Lower voltage, but higher current
  - Joule heating is $I^2R$

- Has resulted in less robust package designs

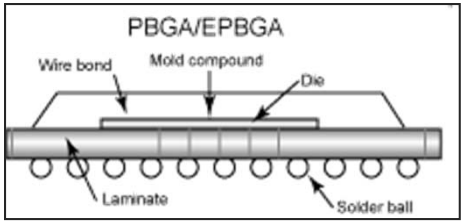
# Solder Wearout (cont.)

- Elimination of leaded devices
  - Provides lower resistance-capacitance (RC) and higher package densities
  - Reduces compliance

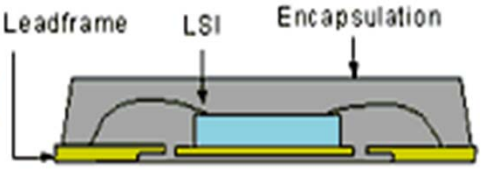
Cycles to failure
-40 to 125C



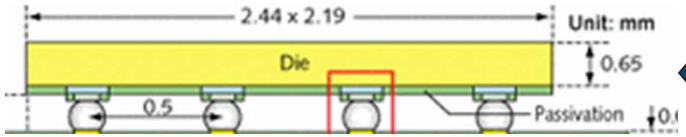

QFP: >10,000




BGA: 3,000 to 8,000




QFN: 1,000 to 3,000




CSP / Flip Chip: <1,000

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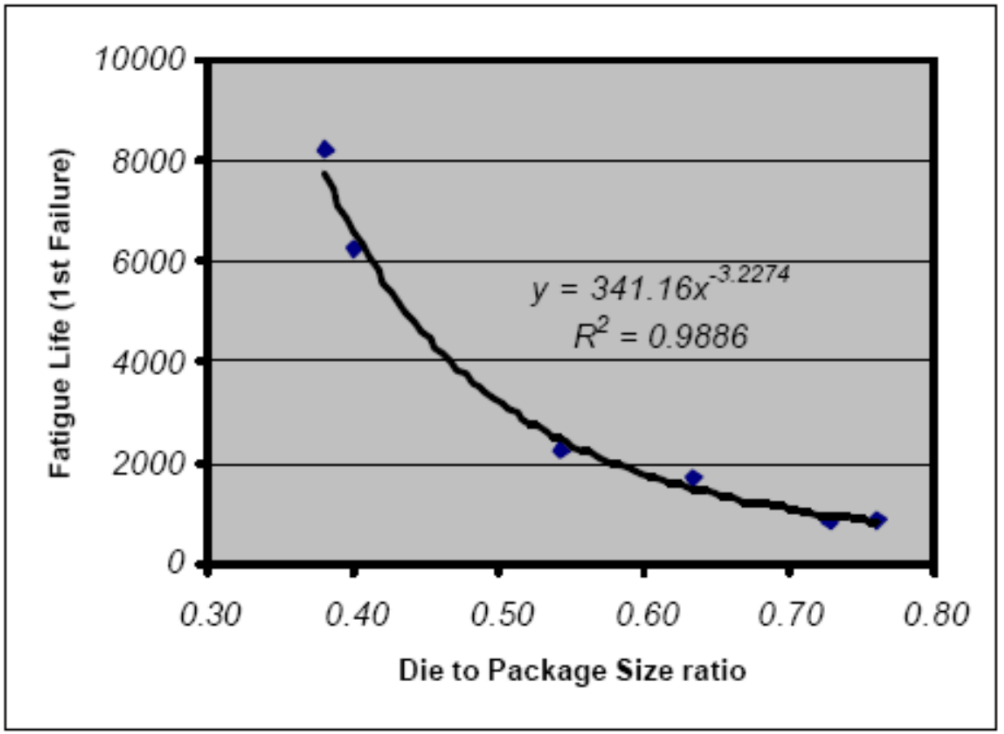
# Solder Wearout (cont.)

- Design change: More silicon, less plastic
- Increases mismatch in coefficient of thermal expansion (CTE)



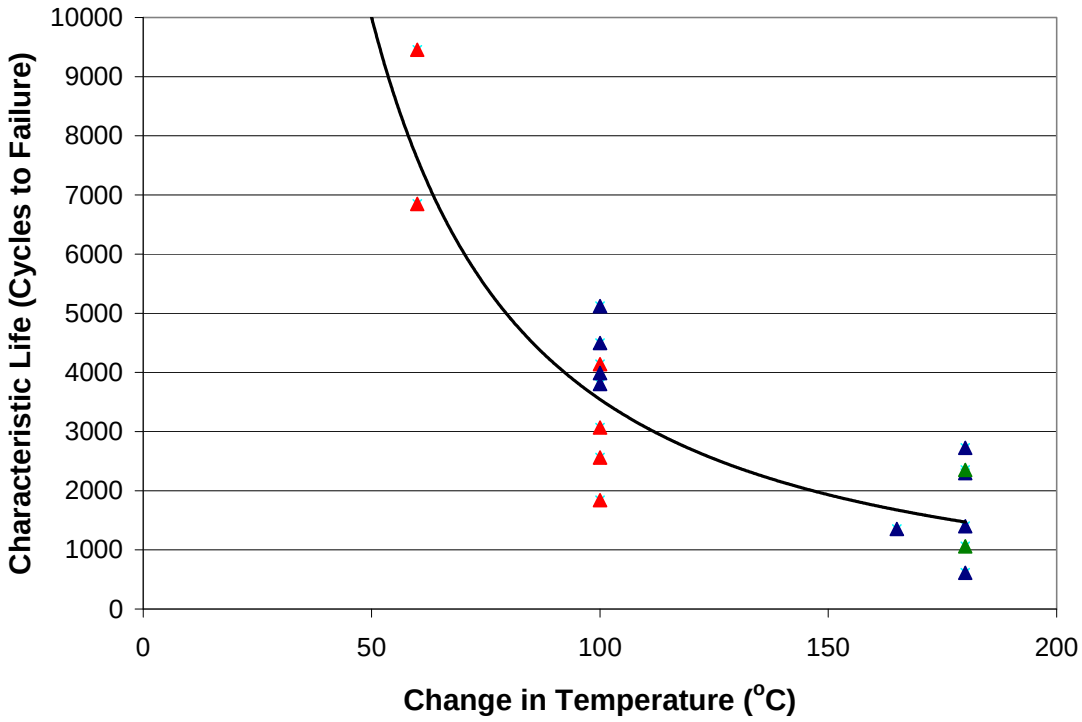

BOARD LEVEL ASSEMBLY AND RELIABILITY CONSIDERATIONS FOR QFN TYPE PACKAGES, Ahmer Syed and WonJoon Kang, Amkor Technology.

# Solder Wearout (cont.)

- Hotter devices
  - Increases change in temperature ($\Delta T$)

$$t_f = \Delta T^n$$

n = 2 (SnPb)
n = 2.3 (SnNiCu)
n = 2.7 (SnAgCu)

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# Industry Response to SJ Wearout?

- JEDEC
  - Specification body for component manufacturers
- JEDEC JESD47
  - Guidelines for new component qualification
  - Requires **2300** cycles of 0 to 100C
  - Testing is often done on thin boards
- IPC
  - Specification body for electronic OEMs
- IPC 9701
  - Recommends **6000** cycles of 0 to 100C
  - Test boards should be similar thickness as actual design

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# BIG PROBLEM

- JEDEC requirements are 60% less than IPC
- Testing on a thin board can extend lifetimes by 2X to 4X

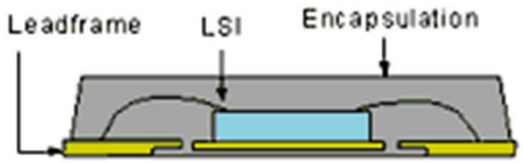
- What does this mean?
  - The components you buy may only survive 500 cycles of 0 to 100C

- What must you do?
  - Components at risk must be subjected to PoF-based (Physics of Failure) reliability analysis

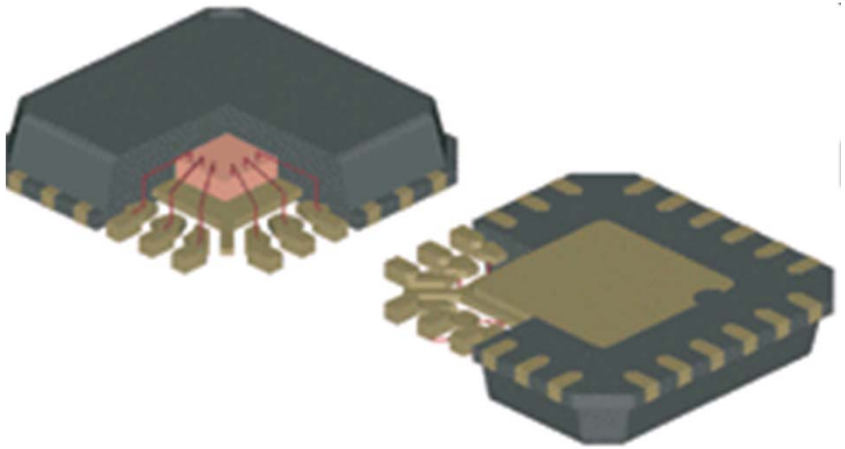
# Quad Flat Pack No Leads or Quad Flat No Leads (QFN)

# QFN: What is it?

- **Q**uad **F**lat Pack **N**o Lead or **Q**uad **F**lat **N**on-Leaded
  - 'The poor man's ball grid array'
  - Also known as
    - Leadframe Chip Scale Package (LF-CSP)
    - MicroLeadFrame (MLF)
    - Others (MLP, LPCC, QLP, HVQFN, etc.)




- Overmolded leadframe with bond pads exposed on the bottom and arranged along the periphery of the package
  - Developed in the early to mid-1990's by Motorola, Toshiba, Amkor, etc.
  - Standardized by JEDEC/EIAJ in late-1990's
  - Fastest growing package type



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# QFN Advantages: Size and Cost

- Smaller, lighter and thinner than comparable leaded packages
  - Allows for greater functionality per volume
- Reduces cost
  - Component manufacturers: More ICs per frame
  - OEMs: Reduced board size
- Attempts to limit the footprint of lower I/O devices have previously been stymied for cost reasons
  - BGA materials and process too expensive

# Advantages: Manufacturability

- Small package without placement and solder printing constraints of fine pitch leaded devices
  - No special handling/trays to avoid bent or non planar pins
  - Easier to place correctly on PCB pads than fine pitch QFPs, TSOPs, etc.
  - Larger pad geometry makes for simpler solder paste printing
  - Less prone to bridging defects when proper pad design and stencil apertures are used.
- Reduced popcorning moisture sensitivity issues – smaller package

# Advantages: Thermal Performance

- More direct thermal path with larger area
  - Die → Die Attach → Thermal Pad → Solder → Board Bond Pad
- θJa for the QFN is about half of a leaded counterpart (as per JESD-51)
  - Allows for 2X increase in power dissipation

| Package Type | Body Size (mm) | Leads | Height (mm) | Max Die Size | PCB Area | θ Ja |
|---|---|---|---|---|---|---|
| QFN | 7 x 7 | 48 | 1.00 max | 203 x 203 mils | 49 mm² | 27 |
| TQFP | 7 x 7 | 48 | 1.20 max | 190 x 190 mils | 81 mm² | 55 |
| QFN | 5 x 7 | 38 | 1.00 max | 124 x 202 mils | 35 mm² | 34 |
| TSSOP | 4.4 x 9.7 | 38 | 1.10 max | 108 x 207 mils | 62 mm² | 73 |
| QFN | 5 x 5 | 16 | 1.00 max | 124 x 124 mils | 25 mm² | 37 |
| QSOP | 3.9 x 4.9 | 16 | 1.75 max | 86 x 120 mils | 31 mm² | 112 |

# Advantages: Inductance

- At higher operating frequencies, inductance of the gold wire and long lead-frame traces will affect performance
- Inductance of QFN is half its leaded counterpart because it eliminates gullwing leads and shortens wire lengths

**Popular for RF Designs**

Table 1. Comparison of inductance components for a QFN and SOIC.

| | Inductance (nH) | |
|---|---|---|
| Package | QFN 7 mm, 48 Lead | TQFP 7 mm, 48 Lead |
| Die size | 4.5 x 4.5 mm | 4.25 x 4.25 mm |
| Center lead | 0.067 | 0.871 |
| Center wire | 0.867 | 0.837 |
| Center total (lead + wire) | **0.934** | **1.708** |
| Corner lead | 0.085 | 1.010 |
| Corner wire | 1.081 | 0.964 |
| Corner total (lead + wire) | **1.166** | **1.974** |

http://ap.pennnet.com/display_article/153955/36/ARTCL/none/none/1/The-back-end-process:-Step-9-QFN-Singulation/

# QFN: Why Not?

- QFN is a 'next generation' technology for non-consumer electronic OEMs due to concerns with
  - Manufacturability
  - Compatibility with other OEM processes
  - Reliability
- Acceptance of this package, especially in long-life, severe environment, high-rel applications, is currently limited as a result

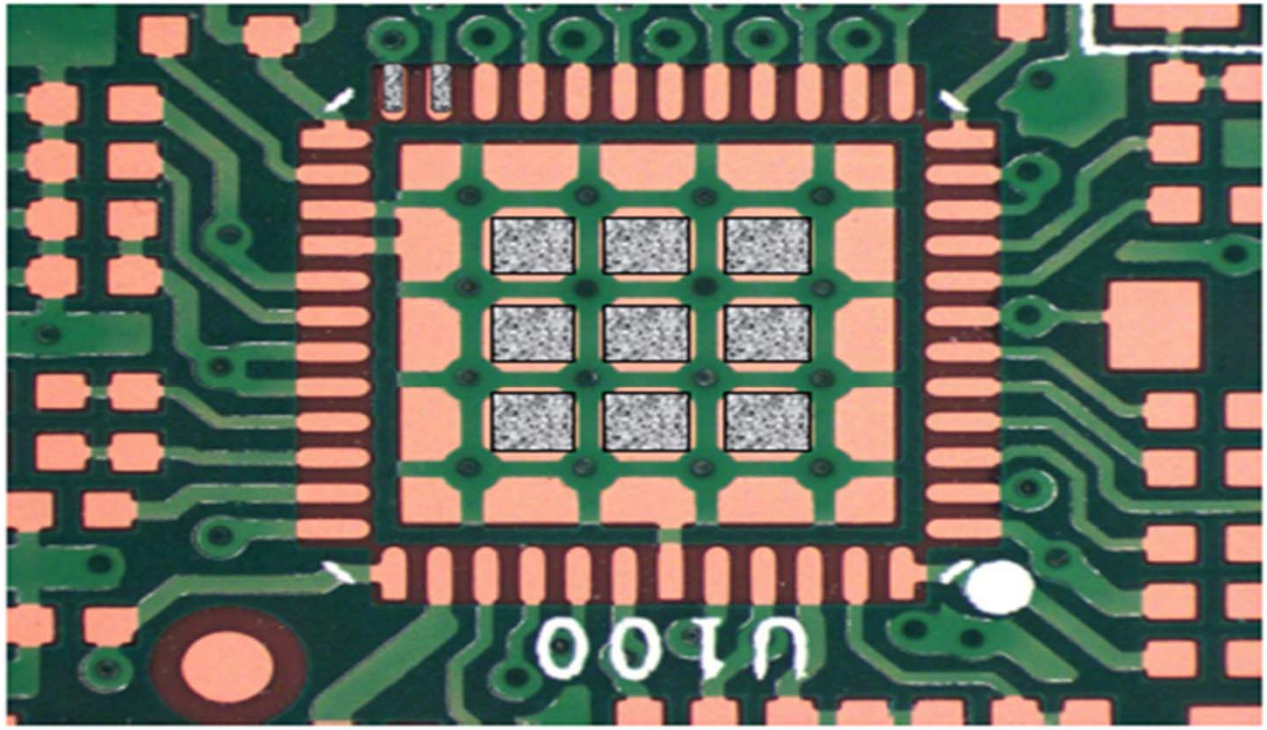
# QFN Manufacturability: Bond Pads

- Non Solder Mask Defined Pads Preferred (NSMD)
  - Copper etch process has tighter process control than solder mask process
  - Makes for more consistent, strong solder joints since solder bonds to both tops and sides of pads
- Use solder mask defined pads (SMD) with care
  - Can be used to avoid bridging between pads, especially between thermal and signal pads.
  - Pads can grow in size quite a bit based on PCB mfg capabilities
- Can lose solder volume and standoff height through vias in thermal pads
  - May need to tent, plug, or cap vias to keep sufficient paste volume
  - Reduced standoff weight reduces cleanability and pathways for flux outgassing
    - Increased potential for contamination related failures
  - Tenting and plugging vias is often not well controlled and can lead to placement and chemical entrapment issues
  - Exercise care with devices placed on opposing side of QFN
  - Can create placement issues if solder "bumps" are created in vias
  - Can create solder short conditions on the opposing device
  - Capping is a more robust, more expensive process that eliminates these concerns

# Increase component standoff through PCB design

- One option: Soldermask Lift

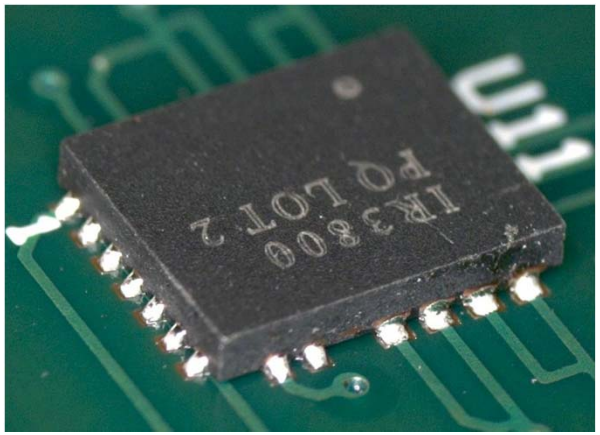
A solution to the QFN entrapment problem is the "Soldermask Lift" to allow for proper venting for a no clean or cleanability with the water soluble solderpaste residues. Current designs only create a 0.5 to 1.0 mil standoff but the Soldermask Lift will create a 3-4 mil standoff.



By placing soldermask plugs in the thermal vents on the ground plan and then putting strips over the plugs and creating a windowpane area for soldermask which create less flux and more open space for the solder to lift the part up. Only place solder paste in the marked areas to reduce the flux but it will still give you similar and effective thermal dissipation. Then place solderpaste on the pads.

# Bond Pads (cont.)

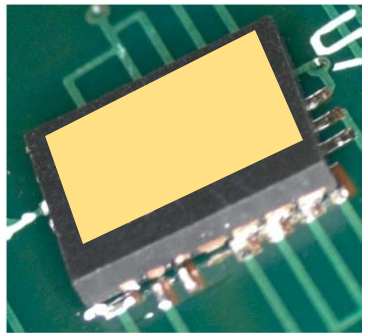
- Extend bond pad 0.2 – 0.3 mm beyond package footprint
  - May or may not solder to cut edge
  - Allows for better visual inspection

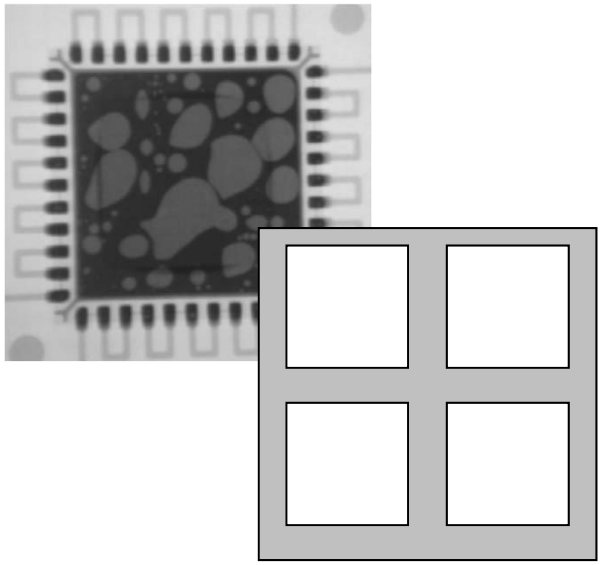



- Really need X-ray for best results
  - Allows for verification of bridging, adequate solder coverage and void percentage
  - Note: Lacking in good criteria for acceptable voiding

# Manufacturability: Stencil Design

- Stencil thickness and aperture design can be crucial for manufacturability
  - Excessive amount of paste can induce float, lifting the QFN off the board
  - Excessive voiding can also be induced through inappropriate stencil design
- Follow manufacturer's guidelines
  - Goal is 2-3 mils of solder thickness
- Rules of thumb (thermal pad)
  - Ratio of aperture/pad ~0.5:1
  - Consider multiple, smaller apertures (avoid large bricks of solder paste)
  - Reduces propensity for solder balling





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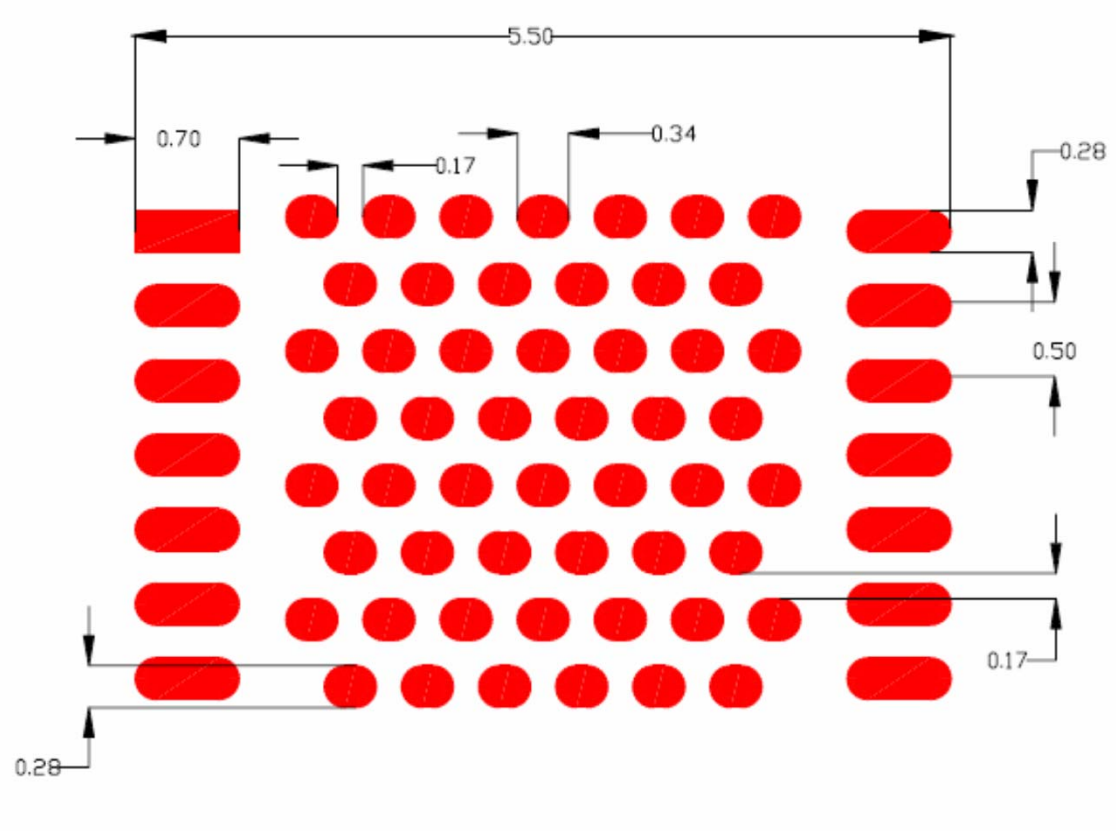
# Manufacturability: Stencil Design

Datasheet says solder paste coverage should be 40-80%




Drawing supplied in same datasheet is for 26% coverage

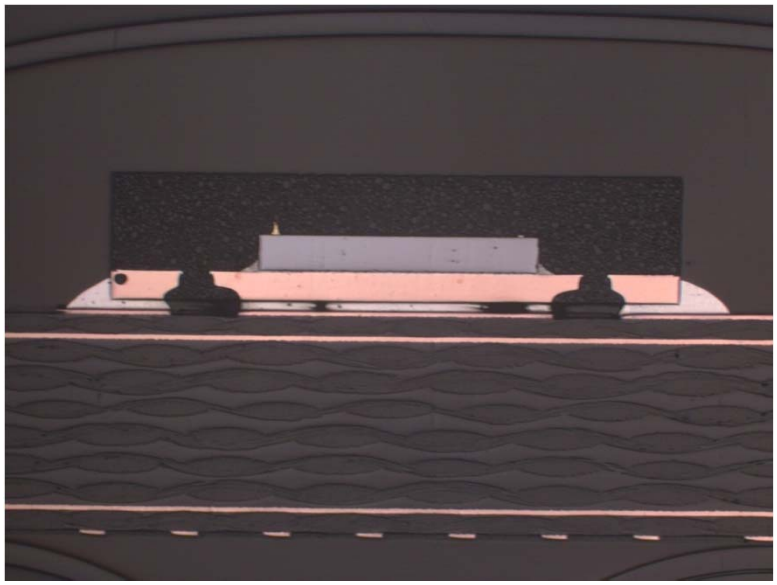
# Manufacturability: Reflow & Moisture

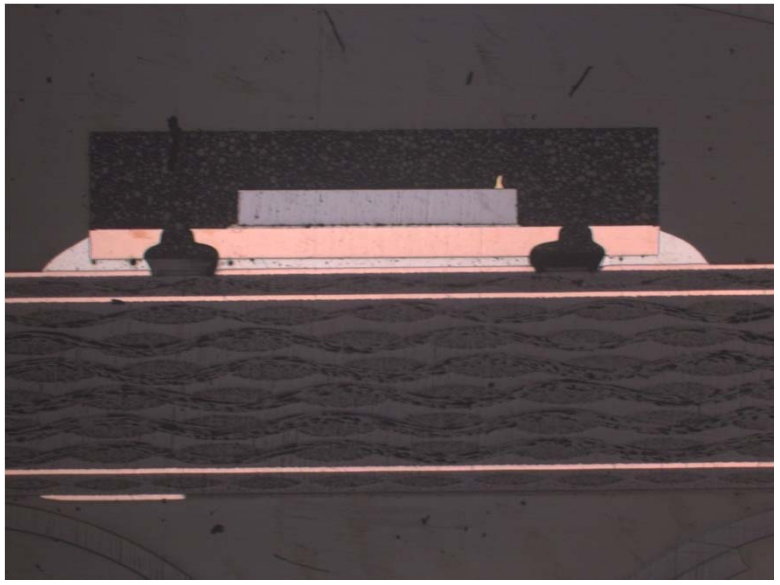
- QFN solder joints are more susceptible to dimensional changes
- Case Study: Military supplier experienced solder separation under QFN
- QFN supplier admitted that the package was more susceptible to moisture absorption that initially expected
  - Resulted in transient swelling during reflow soldering
  - Induced vertical lift, causing solder separation
- Was **not** popcorning
  - No evidence of cracking or delamination in component package

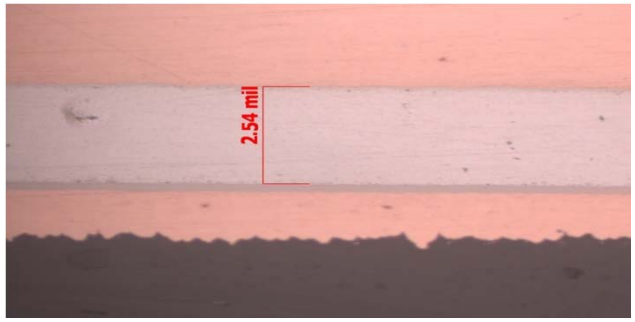
# Corrective Actions: Manufacturing

- Verify good MSL handling/procedures
- Spec and confirm - Reflow
  - Room temperature to preheat (max 2-3°C/sec)
  - Preheat to at least 150°C
  - Preheat to maximum temperature (max 4-5°C/sec)
  - Cooling (max 2-3°C/sec)
    - In conflict with profile from J-STD-020C (6°C/sec)
  - Make sure assembly is less than 60°C before cleaning

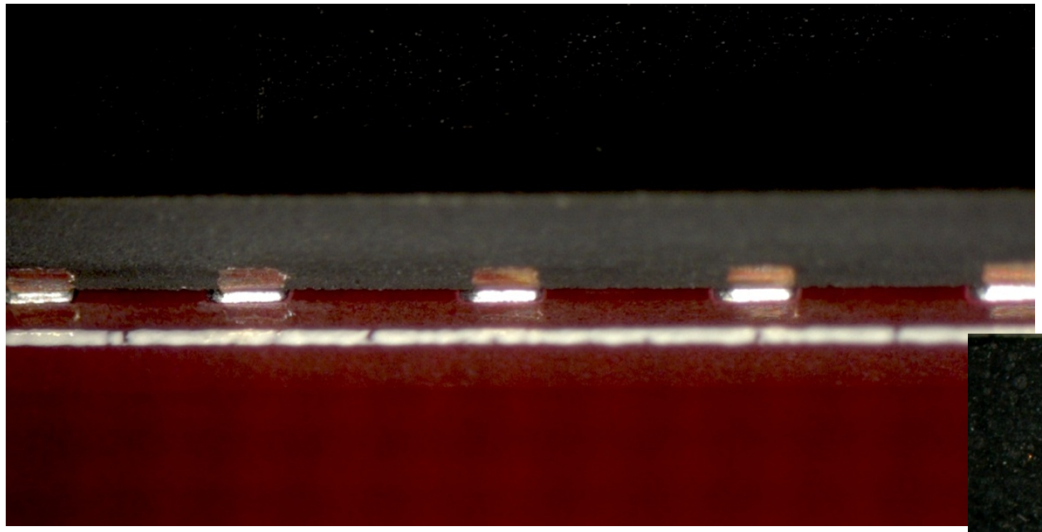
# Manufacturability: QFN Joint Inspection

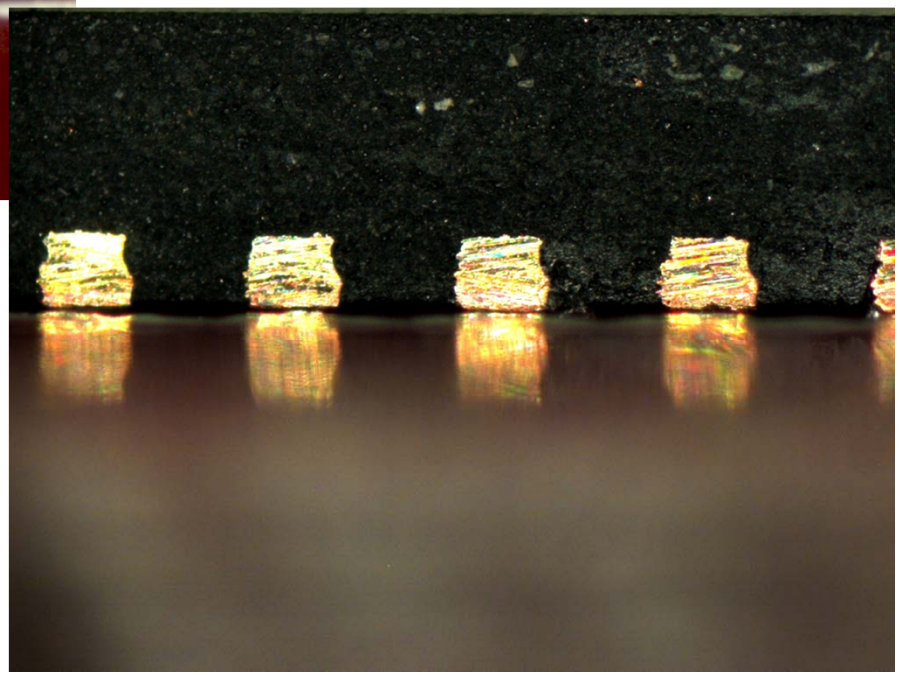






# Manufacturability: QFN Joint Inspection





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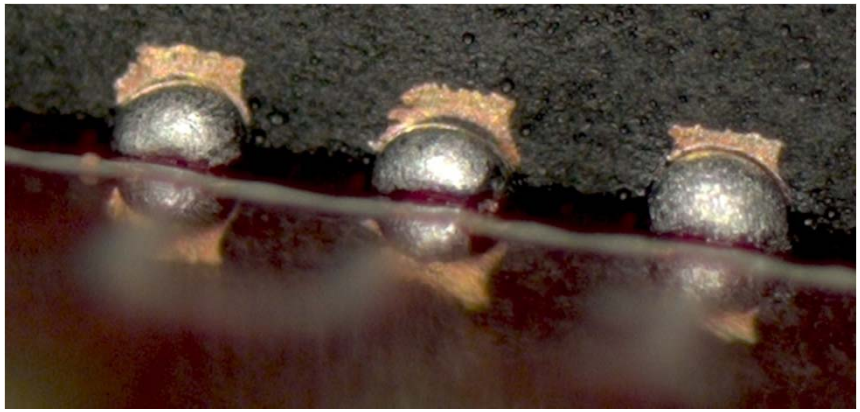
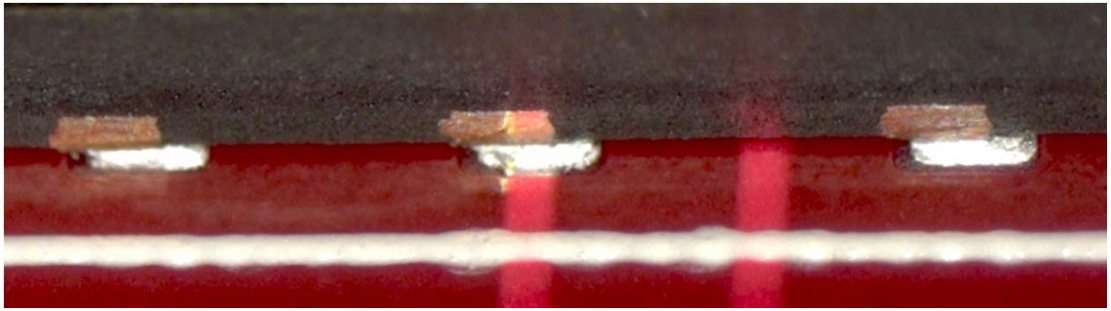


Convex or absence of fillet highly likely

- Etching of leadframe can prevent pad from reaching edge of package
- Edge of bond pad is not plated for solderability



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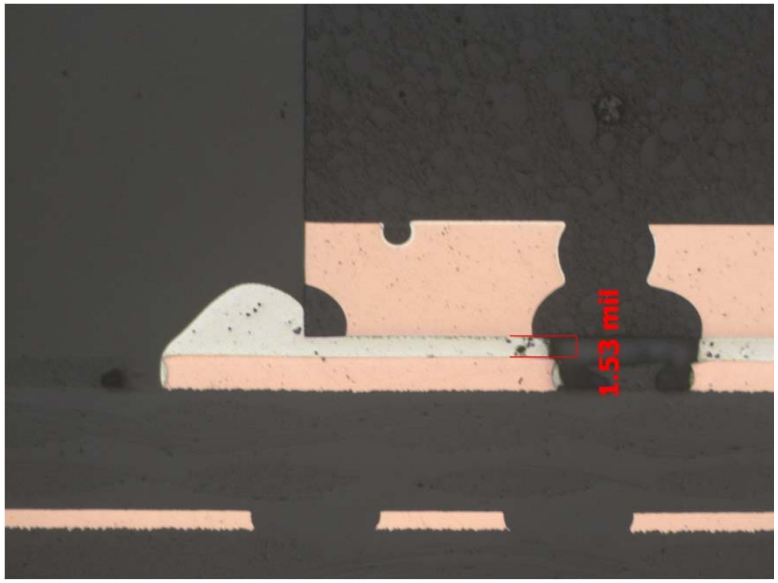
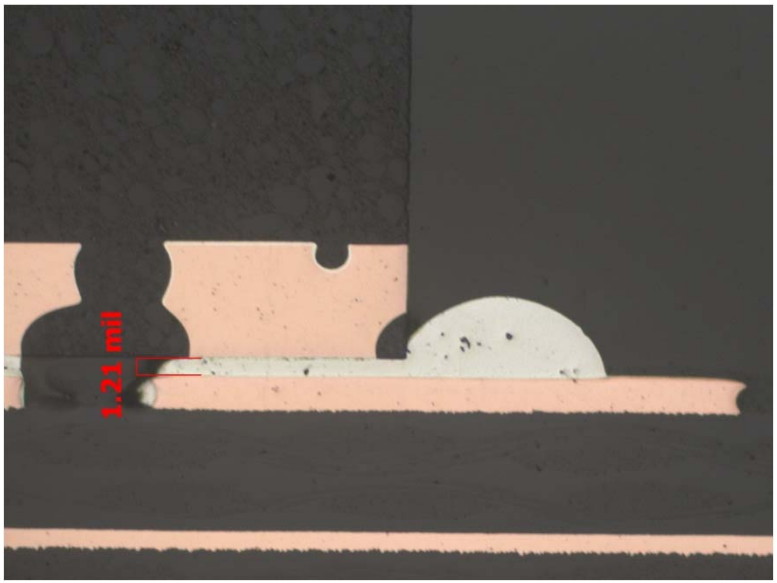



- A large convex fillet is often an indication of issues
  - Poor wetting under the QFN
  - Tilting due to excessive solder paste under the thermal pad
  - Elevated solder surface tension, from insufficient solder paste under the thermal pad, pulling the package down

# Manufacturability: Rework

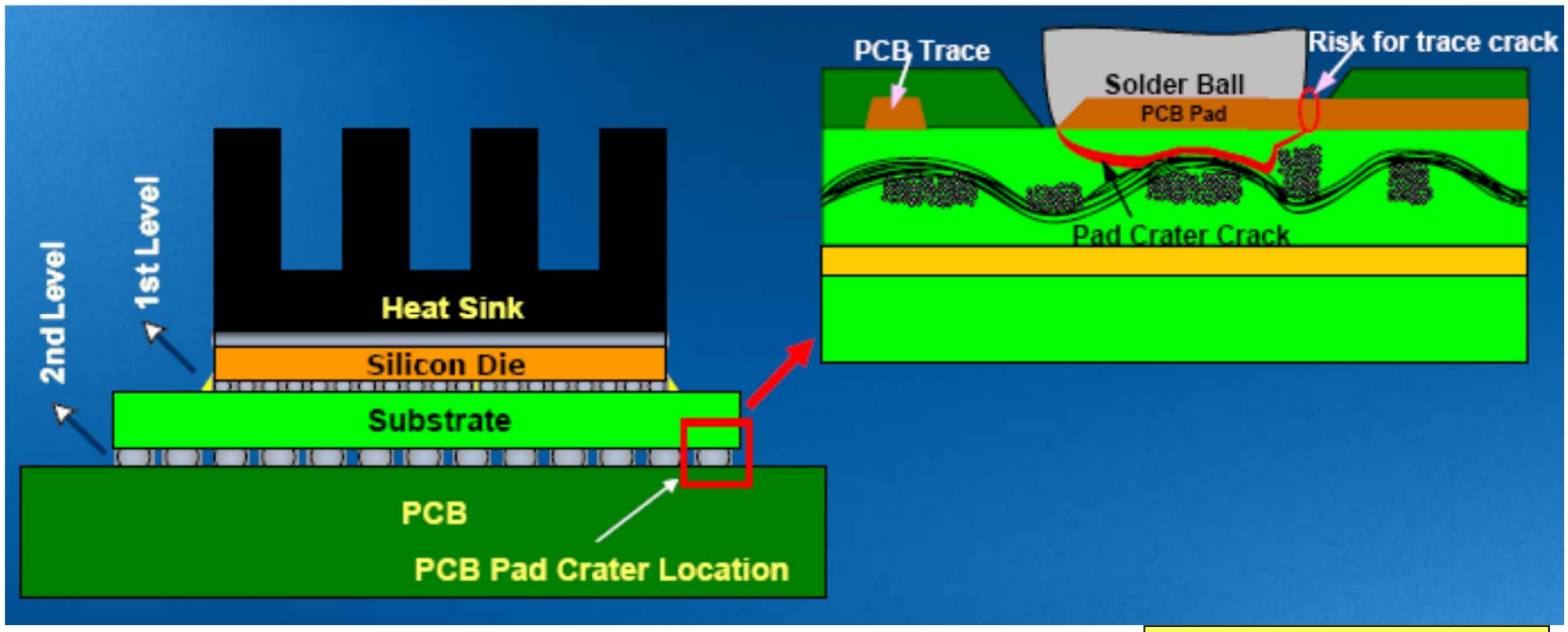
- Can be difficult to replace a package and get adequate soldering of thermal / internal pads.
  - Mini-stencils, preforms, or rebump techniques can be used to get sufficient solder volume
- Not directly accessible with soldering iron and wire
  - Portable preheaters used in conjunction with soldering iron can simplify small scale repair processes
- Close proximity with capacitors often requires adjacent components to be resoldered / replaced as well

# Manufacturability: Board Flexure

- Area array devices are known to have board flexure limitations
  - For SAC attachment, maximum microstrain can be as low as 500 με
- QFN has an even lower level of compliance
  - Limited quantifiable knowledge in this area
  - Must be conservative during board build
  - IPC is working on a specification similar to BGAs

# Pad Cratering

- Cracking initiating within the laminate during a dynamic mechanical event
  - In circuit testing (ICT), board depanelization, connector insertion, shock and vibration, etc.

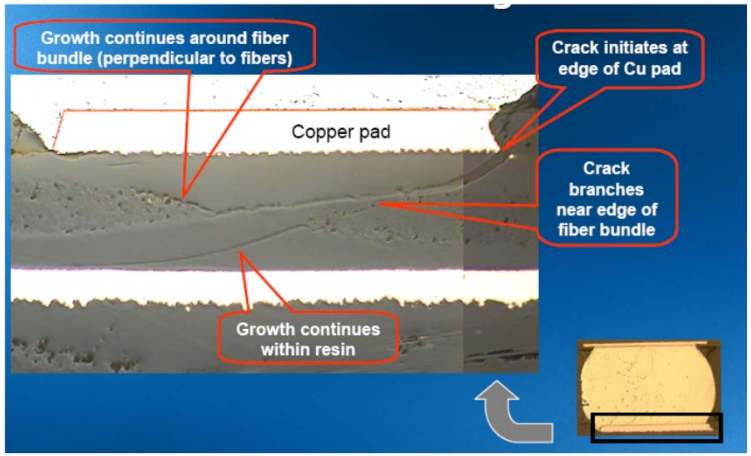



G. Shade, Intel (2006)

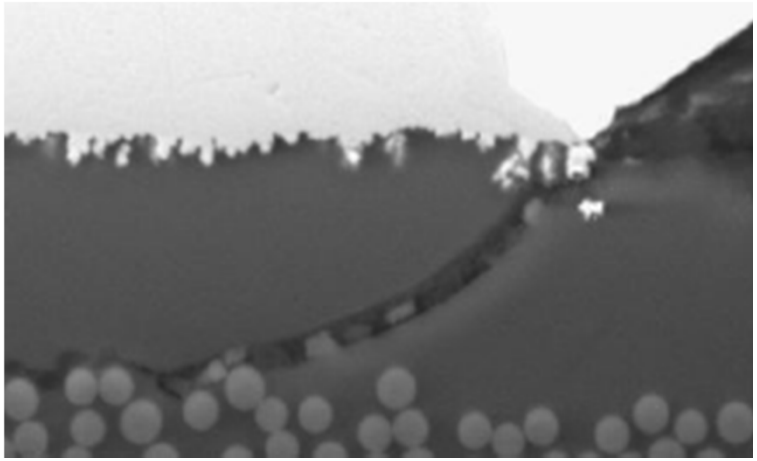
# Pad Cratering

- Drivers
  - Finer pitch components
  - More brittle laminates
  - Stiffer solders (SAC vs. SnPb)
  - Presence of a large heat sink

Intel (2006)




- Difficult to detect using standard procedures
  - X-ray, dye-n-pry, ball shear, and ball pull

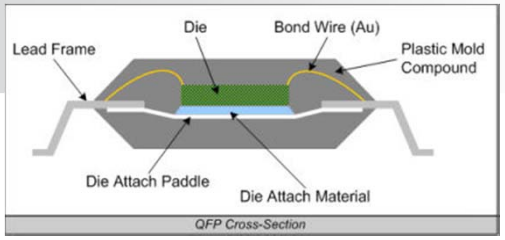


# Solutions to Pad Cratering

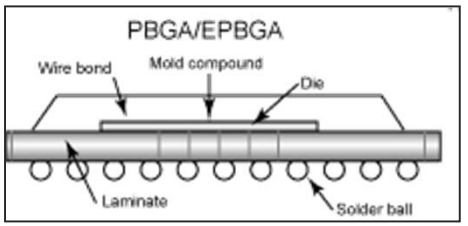
- Board Redesign
  - Solder mask defined vs. non-solder mask defined
- Limitations on board flexure
  - 750 to 500 microstrain, Component dependent
- More compliant solder
  - SAC305 is relatively rigid, SAC105 and SNC are possible alternatives
- New acceptance criteria for laminate materials
  - Intel-led industry effort
  - Attempting to characterize laminate material using high-speed ball pull and shear testing, Results inconclusive to-date
- Alternative approach
  - Require reporting of fracture toughness and elastic modulus

# Reliability: Thermal Cycling

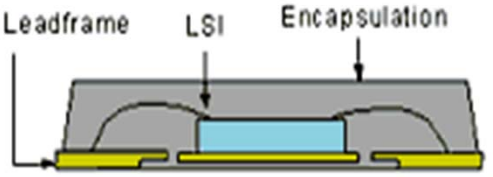
- Order of magnitude reduction in time to failure from QFP
  - 3X reduction from BGA
- Driven by die / package ratio
  - 40% die; tf = 8K cycles (-40 / 125C)
  - 75% die; tf = 800 cycles (-40 / 125C)
- Driven by size and I/O#
  - 44 I/O; tf = 1500 cycles (-40 / 125C)
  - 56 I/O; tf = 1000 cycles (-40 / 125C)
- Very dependent upon solder bond with thermal pad




QFP: >10,000




BGA: 3,000 to 8,000




QFN: 1,000 to 3,000

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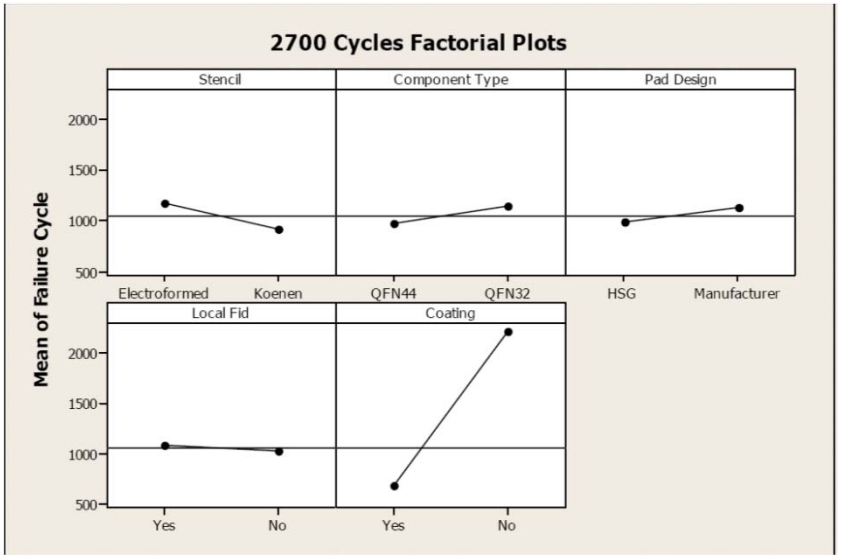
# Thermal Cycling: Conformal Coating

- Care must be taken when using conformal coating over QFN
  - Coating can infiltrate under the QFN
  - Small standoff height allows coating to cause lift
- Hamilton Sundstrand found a significant reduction in time to failure (-55 / 125C)
  - Uncoated: 2000 to 2500 cycles
  - Coated: 300 to 700 cycles
- Also driven by solder joint sensitivity to tensile stresses
  - Damage evolution is far higher than for shear stresses




Wrightson, SMTA Pan Pac 2007

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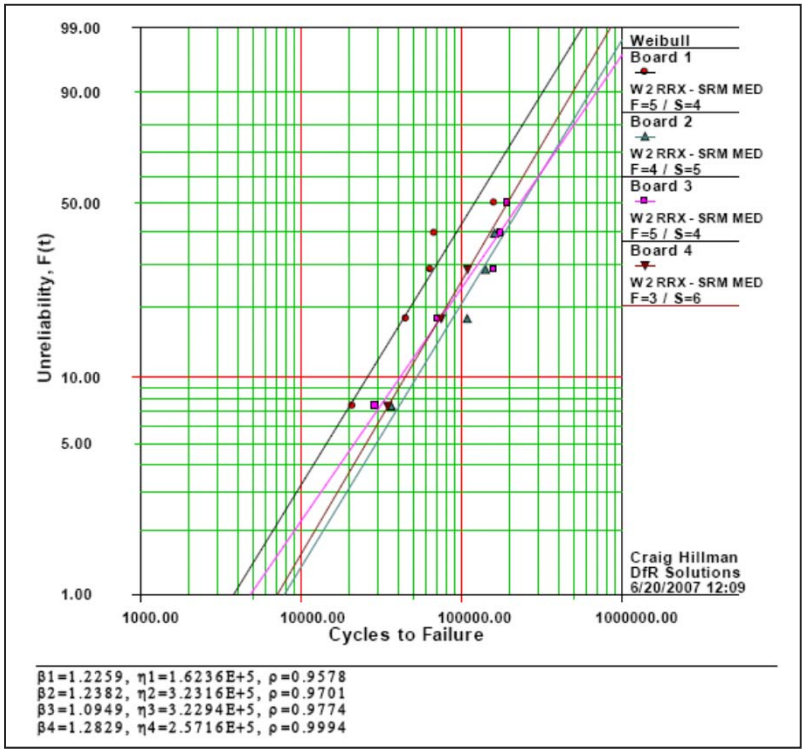
# Reliability: Bend Cycling

- Low degree of compliance and large footprint can also result in issues during cyclic flexure events




- Example: IR tested a 5 x 6mm QFN to JEDEC JESD22-B113
  - Very low beta (~1)
  - Suggests brittle fracture, possible along the interface

# Reliability: Dendritic Growth / Electrochemical Migration

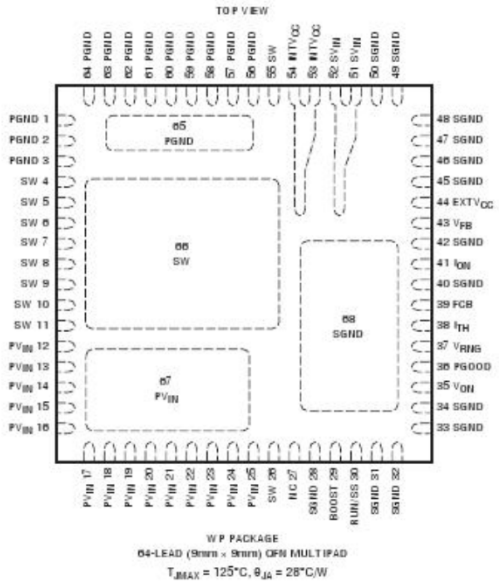
- Large area, multi-I/O and low standoff can trap flux under the QFN
- Processes using no-clean flux should be requalified
  - Particular configuration could result in weak organic acid concentrations above maximum (150 – 200 ug/in$^2$)
- Those processes not using no-clean flux will likely experience dendritic growth without modification of cleaning process
  - Changes in water temperature
  - Changes in saponifier
  - Changes to impingement jets

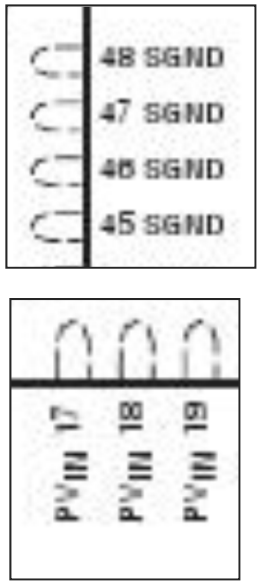
# Dendritic Growth (cont.)

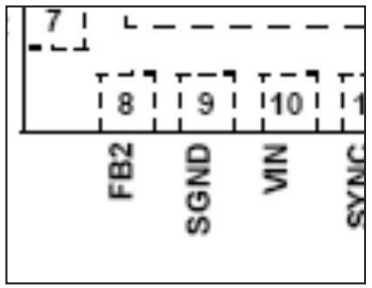
- The electric field strength between adjacent conductors is a strong driver for dendritic growth
  - Voltage / distance
- Digital technology typically has a maximum field strength of 0.5 V/mil
  - TSSOP80 with 3.3VDC power and 16 mil pitch
- Previous generation analog / power technology had a maximum field strength of 1.6 V/mil
  - SOT23 with 50VDC power and 50 mil pitch
- Introduction of QFN has resulted in electric fields as high as 3.5 V/mil
  - 24VDC and 16 mil pitch

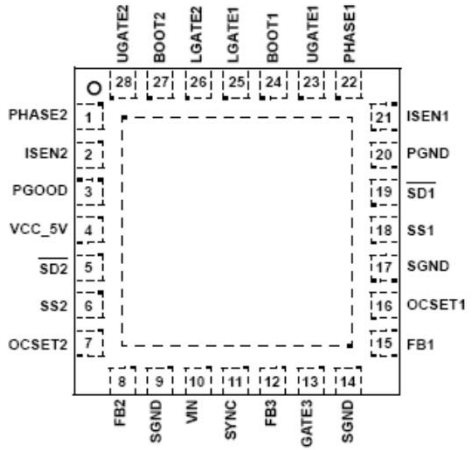
# Dendritic Growth (cont.)

- Component manufacturers are increasingly aware of this issue and separate power and ground
  - Linear Technologies (left) has strong separation power and ground
  - Intersil (right) has power and ground on adjacent pins

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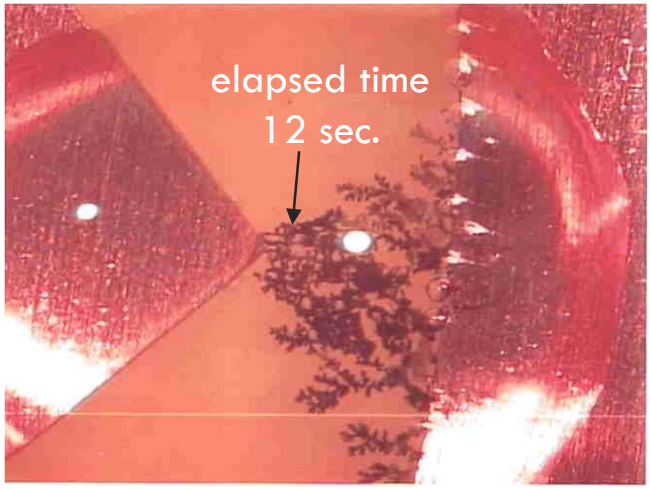
# Electro-Chemical Migration: Details



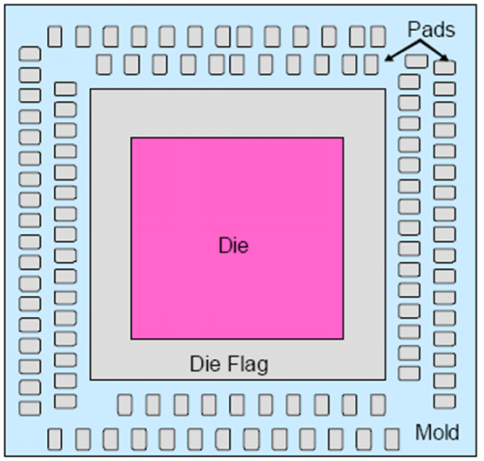

- Insidious failure mechanism
  - Self-healing: leads to large number of no-trouble-found (NTF)
  - Can occur at nominal voltages (5 V) and room conditions (25C, 60%RH)
- Due to the presence of contaminants on the surface of the board
  - Strongest drivers are halides (chlorides and bromides)
  - Weak organic acids (WOAs) and polyglycols can also lead to drops in the surface insulation resistance
- Primarily controlled through controls on cleanliness
  - Minimal differentiation between existing Pb-free solders, SAC and SnCu, and SnPb
  - Other Pb-free alloys may be more susceptible (e.g., SnZn)

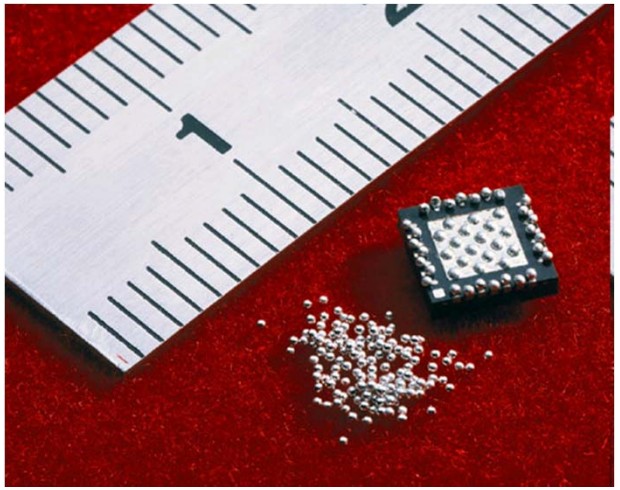
## Cleanliness Recommendations

| Ion | Control | Maximum |
|---|---|---|
| Fluoride | N/A | 1 μg/in$^2$ |
| Chloride | 2 μg/in$^2$ | 4.5 μg/in$^2$ |
| Bromide | 10 μg/in$^2$ | 15 μg/in$^2$ |
| Nitrates, Sulfates | 2 – 4 μg/in$^2$ | 6 – 12 μg/in$^2$ |
| WOAs | 150 μg/in$^2$ | 250 μg/in$^2$ |

# QFN: Risk Mitigation

- Assess manufacturability
  - DOE on stencil design
  - Degree of reflow profiling
  - Control of board flexure
  - Dual row QFN is especially difficult
  - Cleanliness is critical
- Assess reliability
  - Ownership of 2nd level interconnect is often lacking
  - Extrapolate to needed field reliability
  - Some companies have reballed QFN to deal with concerns



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Thank you!

Any Questions?

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*Dr. Craig Hillman, CEO*

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